P3-ROC

P3 – Remote Operations Controller

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Version 1.2 – Aug 27, 2015

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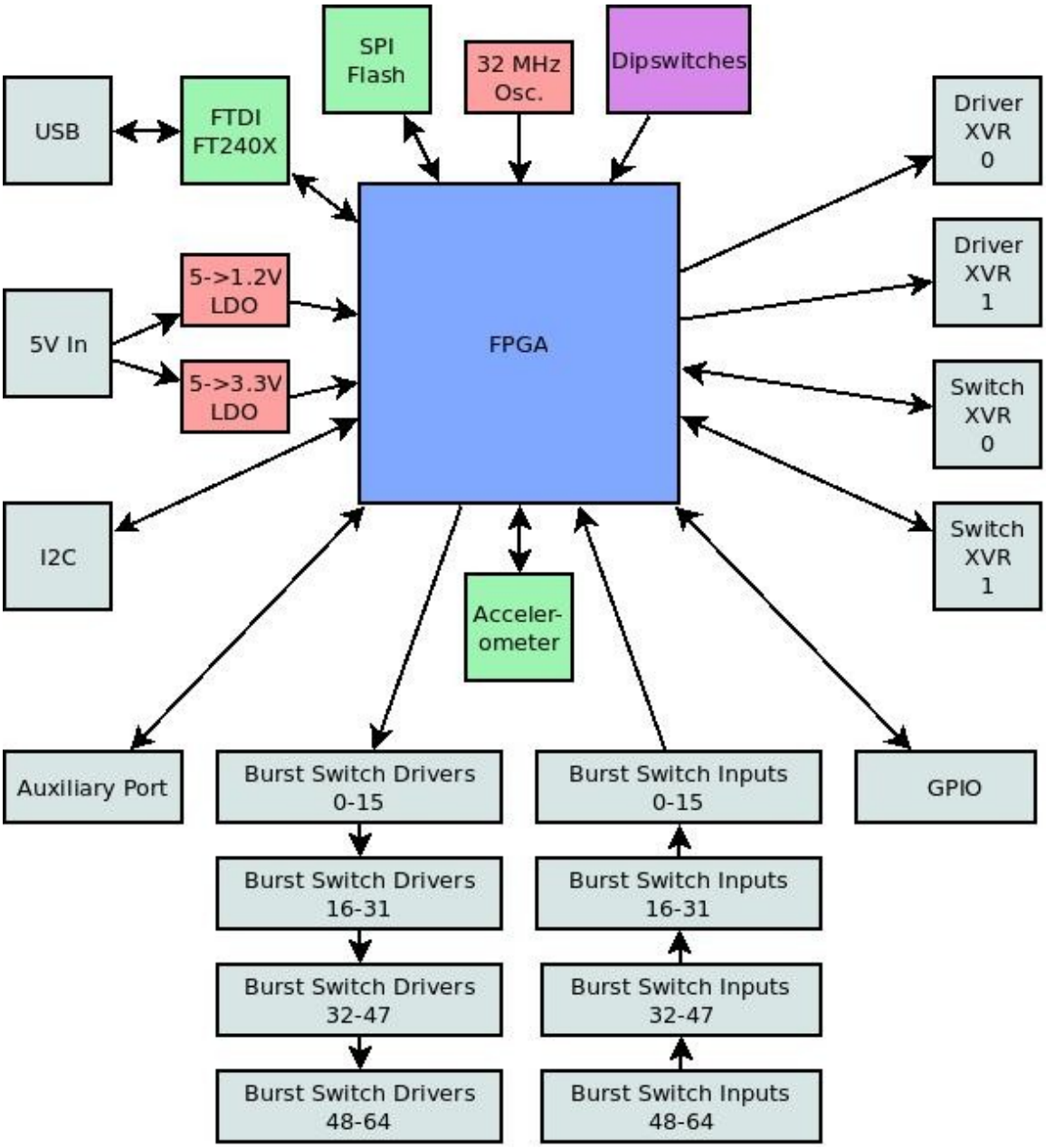
1 Introduction

The P3-ROC is designed to control all of the real-time signaling features on a pinball machine. Major functionality includes:

- Communication with a host processor via USB
- 2 serial switch board interfaces
  - Monitor and react to switch events from 256 switches via serial switch boards
  - Allow host to read switch states from 1024 switches via serial switch boards
- 64 individual burst switches for frequency controlled IR devices
- 2 serial driver board interfaces
  - Control 256 matrixed or direct drivers on serial driver boards with the following functions:
    - On/Off, Pulse, Schedule, Patter, Pulsed-Patter
  - Pass software commands directly to serial driver boards
- 3-axis accelerometer
- Software accessible I2C interface.
- 8-data / 8-control auxiliary bus with microcode engine
- 8 general purpose I/Os (3.3v)

2 Block Diagram



3 Theory of Operation

The P3-ROC consists primarily of an FPGA, supporting logic, and a bunch of connectors. The FPGA is responsible for driving all of the real-time signaling features on a pinball machine. Upon power-up, the FPGA receives its default configuration from an onboard SPI Flash. It then waits for additional configuration information from a host software program over the USB bus.

The USB signaling is handled by an FTDI FT240X device, which has a FIFO interface connected to the FPGA. All information delivered to the FPGA is held in the FIFO until the FPGA reads it. Similarly, all data written into the FIFO by the FPGA is held until the host requests it.

Once configured by the host software program, the FPGA continuously performs functions such as requesting data from the serial switch chains and reacting to switch state changes, writing driver data through the serial driver chain, requesting accelerometer data and responding to accelerometer interrupts, writing burst switch data to the burst switch drivers, and receiving burst switch data from the burst switch inputs. The FPGA can also be used to communicate with an external I2C device and read/write to memory locations in the SPI flash.

4 Functional Descriptions

4.1 USB

A USB interface is used to connect the P-ROC to a host computer. Connectivity is provided with a type-B USB connector, and the signaling is controlled by an FTDI FT240X device. The FTDI chip's FIFO (first-in first-out memory) is connected to the FPGA, which can read data from and write data into the FIFO.

4.2 Burst Switches

All 64 burst drivers and 64 burst inputs are connected directly to the FPGA. The drivers can be configured in the FPGA to drive a certain number of pulses, each a configurable number of microseconds, before turning off for another configurable number of microseconds. This functionality is necessary to enable frequency tuned infrared receivers to accurately receive infrared light from the pulsed emitters.

4.3 Serial Switches

The P3-ROC provides two connectors for serial switch board chains. Both connectors are driven with the same information. Every millisecond, the FPGA automatically requests switch data from 16 serial switch board addresses (2 registers representing 8 switches each per address). Therefore 256 switches are automatically scanned by the FPGA.

Host software can read specific addresses from specific switch boards at any time by issuing register read requests. Available destination switch board address are 0-63.

4.4 Serial Drivers

Drivers are used to send on/off signals to devices through serial driver boards. The P3-ROC provides two connectors for serial driver board chains. Both connectors are driven with the same information.

The FPGA can automatically drive up to 256 drivers, each of which can be configured to operate independently or as part of a matrix. There are no drive outputs on the P3-ROC itself. Rather, they must be connected to the P3-ROC via the serial driver board connectors.

The FPGA provides convenience functions for each driver, thereby freeing up host software from the low level details for each driver. Convenience functions include:

- On/off – Drivers can be configured to be on until they are reconfigured to be off.
- Pulse – Drivers can be configured to be on for a specific number of milliseconds before turning off.
- Schedule – Drivers can be configured to turn on at scheduled times and stay on for a specific number of milliseconds before the schedule is disabled. The scheduled times can be one or more points in time spaced approximately 1/32 of a second apart.
- Patter – Drivers can be configured to repeatedly turn on for a specific number of milliseconds and then off for a specific number of milliseconds.

- Pulsed Patter – Drivers can be configured with a Patter sequence for a specific number of milliseconds before turning off.

4.5 Clocks

Everything runs off of a 32 Mhz Clock.

4.6 Configuration

On power-up, the FPGA, operating in Master Serial mode, automatically loads itself from the SPI Flash. Once loaded, the FPGA waits to be further configured by the host through the USB bus.

If the FPGA ever needs to be updated, it is capable of driving the data pins connected to the SPI Flash. The host software can write an image into the FPGA which will then write the image into the Flash. Note, if this operation begins and does not completely successfully, the image in the Flash will be corrupted. This will keep the FPGA from automatically loading correctly on future power-ups until the Flash is replaced or reprogrammed.

A JTAG header is provided as another way to load the FPGA or to rewrite the image in the Xilinx Platform Flash. Using the JTAG header requires a Xilinx programming cable connected to a computer running Xilinx's programming software.

4.7 Dipswitches

There are 8 dipswitches on the P3-ROC. They are used as follows:

Switch	Function
1	RESERVED
2	RESERVED
3	RESERVED
4	RESERVED
5	RESERVED
6	RESERVED
7	Serial Switch Chain 0 Termination
8	Serial Switch Chain 1 Termination

4.8 Status

There are 2 power leds. When behaving normally, they should all on when the board has power.

LED	Voltage Indication
D50	3.3V
D52	5V

There are 9 LEDs on the board to provide visual indications about the functionality of the board. The LEDs are driven by the FPGA as follows:

LED	Meaning
D3	FPGA initialized properly
D9	FPGA startup completed
D5	32 Mhz clock operational
D8	USB communications established
D7	Watchdog timer expired (Drivers disabled)
D4	Pattern*
D6	Pattern*
D10	Pattern*
D11	Pattern*

* D4, D6, D10, and D11 display a rotating pattern. Normal operation is indicated by a single light rotating counter clockwise.

4.9 Connectors

J1	Power	
4-pin Molex: 0.200” spacing		
1	NC	N/A
2	Ground	I
3	Ground	I
4	VCC (5V)	I

J2	Power	
2-pin Molex: 0.156” spacing		
1	5V	I
2	Ground	I

J3	Burst Switches				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 0	O
3	3.3V	O	4	Burst Switch Driver 1	O
5	Burst Switch Driver 6	O	6	Burst Switch Driver 2	O
7	Ground	O	8	Burst Switch Driver 3	O
9	Ground	O	10	Burst Switch Driver 4	O
11	Ground	O	12	Burst Switch Driver 5	O
13	Burst Switch Driver 7	O	14	Burst Switch Input 0	O
15	Ground	O	16	Burst Switch Input 1	O
17	Ground	O	18	Burst Switch Input 2	O
19	Ground	O	20	Burst Switch Input 3	O
21	Burst Switch Input 7	O	22	Burst Switch Input 4	O
23	3.3V	O	24	Burst Switch Input 5	O
25	3.3V	O	26	Burst Switch Input 6	O

J4	Burst Switches				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 32	O
3	3.3V	O	4	Burst Switch Driver 33	O
5	Burst Switch Driver 38	O	6	Burst Switch Driver 34	O
7	Ground	O	8	Burst Switch Driver 35	O
9	Ground	O	10	Burst Switch Driver 36	O

11	Ground	O	12	Burst Switch Driver 37	O
13	Burst Switch Driver 39	O	14	Burst Switch Input 32	O
15	Ground	O	16	Burst Switch Input 33	O
17	Ground	O	18	Burst Switch Input 34	O
19	Ground	O	20	Burst Switch Input 35	O
21	Burst Switch Input 39	O	22	Burst Switch Input 36	O
23	3.3V	O	24	Burst Switch Input 37	O
25	3.3V	O	26	Burst Switch Input 39	O

J5	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 8	O
3	3.3V	O	4	Burst Switch Driver 9	O
5	Burst Switch Driver 14	O	6	Burst Switch Driver 10	O
7	Ground	O	8	Burst Switch Driver 11	O
9	Ground	O	10	Burst Switch Driver 12	O
11	Ground	O	12	Burst Switch Driver 13	O
13	Burst Switch Driver 15	O	14	Burst Switch Input 8	O
15	Ground	O	16	Burst Switch Input 9	O
17	Ground	O	18	Burst Switch Input 10	O
19	Ground	O	20	Burst Switch Input 11	O
21	Burst Switch Input 15	O	22	Burst Switch Input 12	O
23	3.3V	O	24	Burst Switch Input 13	O
25	3.3V	O	26	Burst Switch Input 14	O

J6	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 40	O
3	3.3V	O	4	Burst Switch Driver 41	O
5	Burst Switch Driver 46	O	6	Burst Switch Driver 42	O
7	Ground	O	8	Burst Switch Driver 43	O
9	Ground	O	10	Burst Switch Driver 44	O
11	Ground	O	12	Burst Switch Driver 45	O
13	Burst Switch Driver 47	O	14	Burst Switch Input 40	O
15	Ground	O	16	Burst Switch Input 41	O
17	Ground	O	18	Burst Switch Input 42	O
19	Ground	O	20	Burst Switch Input 43	O
21	Burst Switch Input 47	O	22	Burst Switch Input 44	O
23	3.3V	O	24	Burst Switch Input 45	O

25	3.3V	O	26	Burst Switch Input 46	O

J7	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 16	O
3	3.3V	O	4	Burst Switch Driver 17	O
5	Burst Switch Driver 22	O	6	Burst Switch Driver 18	O
7	Ground	O	8	Burst Switch Driver 19	O
9	Ground	O	10	Burst Switch Driver 20	O
11	Ground	O	12	Burst Switch Driver 21	O
13	Burst Switch Driver 23	O	14	Burst Switch Input 16	O
15	Ground	O	16	Burst Switch Input 17	O
17	Ground	O	18	Burst Switch Input 18	O
19	Ground	O	20	Burst Switch Input 19	O
21	Burst Switch Input 23	O	22	Burst Switch Input 20	O
23	3.3V	O	24	Burst Switch Input 21	O
25	3.3V	O	26	Burst Switch Input 22	O

J8	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 48	O
3	3.3V	O	4	Burst Switch Driver 49	O
5	Burst Switch Driver 54	O	6	Burst Switch Driver 50	O
7	Ground	O	8	Burst Switch Driver 51	O
9	Ground	O	10	Burst Switch Driver 52	O
11	Ground	O	12	Burst Switch Driver 53	O
13	Burst Switch Driver 55	O	14	Burst Switch Input 48	O
15	Ground	O	16	Burst Switch Input 49	O
17	Ground	O	18	Burst Switch Input 50	O
19	Ground	O	20	Burst Switch Input 51	O
21	Burst Switch Input 55	O	22	Burst Switch Input 52	O
23	3.3V	O	24	Burst Switch Input 53	O
25	3.3V	O	26	Burst Switch Input 54	O

J9	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 24	O
3	3.3V	O	4	Burst Switch Driver 25	O
5	Burst Switch Driver 30	O	6	Burst Switch Driver 26	O

7	Ground	O	8	Burst Switch Driver 27	O
9	Ground	O	10	Burst Switch Driver 28	O
11	Ground	O	12	Burst Switch Driver 29	O
13	Burst Switch Driver 31	O	14	Burst Switch Input 24	O
15	Ground	O	16	Burst Switch Input 25	O
17	Ground	O	18	Burst Switch Input 26	O
19	Ground	O	20	Burst Switch Input 27	O
21	Burst Switch Input 31	O	22	Burst Switch Input 27	O
23	3.3V	O	24	Burst Switch Input 29	O
25	3.3V	O	26	Burst Switch Input 30	O

J10	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 56	O
3	3.3V	O	4	Burst Switch Driver 57	O
5	Burst Switch Driver 62	O	6	Burst Switch Driver 58	O
7	Ground	O	8	Burst Switch Driver 59	O
9	Ground	O	10	Burst Switch Driver 60	O
11	Ground	O	12	Burst Switch Driver 61	O
13	Burst Switch Driver 63	O	14	Burst Switch Input 56	O
15	Ground	O	16	Burst Switch Input 57	O
17	Ground	O	18	Burst Switch Input 58	O
19	Ground	O	20	Burst Switch Input 59	O
21	Burst Switch Input 63	O	22	Burst Switch Input 60	O
23	3.3V	O	24	Burst Switch Input 61	O
25	3.3V	O	26	Burst Switch Input 62	O

J11	**Serial Switches 0**	
3-pin Molex: 0.100” spacing		
1	KEY	N/A
2	Serial Switch Data +	I/O
3	Serial Switch Data -	I/O

J12	**Serial Drivers 0**	
3-pin Molex: 0.100” spacing		
1	Serial Driver Data +	O
2	Serial Driver Data -	O
3	KEY	N/A

J13	USB	
4-pin USB Type B		
1	5B	I
2	Data-	I/O
3	Data+	I/O
4	Ground	I

J14	Serial Switches 1	
3-pin Molex: 0.100” spacing		
1	KEY	N/A
2	Serial Switch Data +	I/O
3	Serial Switch Data -	I/O

J15	Serial Drivers 1	
3-pin Molex: 0.100” spacing		
1	Serial Driver Data +	O
2	Serial Driver Data -	O
3	KEY	N/A

J16	JTAG Port	
14-pin Header: 2mm spacing		
1	Ground	O
2	3.3V	O
3	Ground	O
4	TMS	I
5	Ground	O
6	TCK	I
7	Ground	O
8	TDO	O
9	Ground	O
10	TDI	I
11	Ground	O
12	Ground	O
13	Ground	O
14	Ground	O

J17	I2C	
4-pin Molex: 0.100” spacing		
1	3.3V	O

2	SDA	I/O
3	SCL	I/O
4	Ground	O

J18	Auxiliary Port				
20-pin Header: 0.100” spacing					
1	Ground	O	2	Ground	O
3	Aux Data 0	I/O	4	Aux Control 0	O
5	Aux Data 1	I/O	6	Aux Control 1	O
7	Aux Data 2	I/O	8	Aux Control 2	O
9	Aux Data 3	I/O	10	Aux Control 3	O
11	Aux Data 4	I/O	12	Aux Control 4	O
13	Aux Data 5	I/O	14	Aux Control 5	O
15	Aux Data 6	I/O	16	Aux Control 6	O
17	Aux Data 7	I/O	18	Aux Control 7	O
19	Ground	O	20	Ground	O

J19	GPIO	
10-pin Molex: 0.100” spacing		
1	GPIO 0	I/O
2	GPIO 1	I/O
3	KEY	N/A
4	GPIO 2	I/O
5	GPIO 3	I/O
6	GPIO 4	I/O
7	GPIO 5	I/O
8	GPIO 6	I/O
9	GPIO 7	I/O
10	Ground	O

4.10 Power

There are 2 power connectors for 5V input. Only one should be used at any one time. J1 is pin compatible with a standard personal computer 4-pin power supply cable commonly used to power disk drives. J2 is a simple 2-pin head for 5V and ground.

3.3V is created from the 5V supply using a 3 amp LDO in a DD-PACK package. Components are available from ST Micro, Linear Tech, TI, and National Semi. 3.3V is used by most of the parts on the board. In addition, external burst switch circuitry is expected to use 3.3V from this board.

1.2V is created from the 5V supply using a 300 milliamp LDO in a SOT23-5 package. Components are available from On Semi and Analog Devices. 1.2V is used for the FPGA's core.

5V is optionally used to power the 74HCT244 and 74HCT245 buffers used for the auxiliary bus. Resistor stuff options allow the buffers to alternatively run on 3.3V.